What is claimed is:

1. A method for forming a transistor, comprising:

forming a gate dielectric layer over a portion of a semiconductor substrate, the substrate being substantially free of silicon;

defining a gate electrode over a portion of the gate dielectric layer; and

introducing ions into the substrate proximate the gate electrode to define a source region and a drain region.

2. The method of claim 1, further comprising:

depositing an interlayer dielectric layer over at least part of the gate electrode, the source region, and the drain region;

defining first, second, and third openings in the interlayer dielectric layer over at least part of the gate electrode, the source region, and the drain region; and

depositing a metal into the first, second, and third openings to contact the gate electrode, the source region, and the drain region.

3. The method of claim 1, wherein the substrate comprises a material having a carrier mobility greater than a carrier mobility of silicon.

4. The method of claim 3, wherein the substrate comprises at least one of germanium, indium antimonide, indium phosphide, gallium arsenide, indium arsenide, and lead telluride.

5. The method of claim 1, wherein the gate dielectric comprises a material having a high dielectric constant, the high dielectric constant being at least twice a dielectric constant of silicon dioxide.

6. The method of claim 5, wherein the gate dielectric comprises at least one of aluminum oxide, hafnium oxide, zirconium silicon oxide, strontium titanium oxide, tantalum oxide, barium titanium oxide, zirconium oxide, yttrium oxide, barium strontium titanium oxide, and silicon nitride.

7. The method of claim 1, wherein the gate electrode comprises at least one of titanium nitride, tantalum

nitride, titanium, tantalum, nickel, platinum, polygermanium, and polysilicon.

8. A transistor comprising:

a semiconductor substrate, the substrate being substantially free of silicon; and

a gate dielectric layer formed over a portion of the substrate.

9. The transistor of claim 8, further comprising:

a gate electrode defined over a portion of the gate dielectric layer.

10. The transistor of claim 9, further comprising:

a source region and a drain region proximate the gate electrode, the source and drain regions defined by introduced ions.

11. The transistor of claim 10, further comprising:

an interlayer dielectric layer over at least part of the gate electrode, the source region, and the drain region

12. The transistor of claim 11, wherein the interlevel dielectric defines first, second, and third

openings in the interlayer dielectric layer over at least part of the gate electrode, the source region, and the drain region.

13. The transistor of claim 12, further comprising:

a metal within the first, second, and third openings in contact with the gate electrode, source region, and the drain region.

14. The transistor of claim 8, wherein the substrate comprises a material having a carrier mobility greater than a carrier mobility of silicon.

15. The transistor of claim 14, wherein the substrate comprises at least one of germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, and gallium antimonide.

16. The transistor of claim 8, wherein the gate dielectric comprises a material having a high dielectric constant, the high dielectric constant being greater than the dielectric constant of silicon dioxide.

17. The transistor of claim 16, wherein the gate dielectric comprises at least one of aluminum oxide, hafnium oxide, zirconium silicon oxide, strontium titanium oxide, tantalum oxide, barium titanium oxide, zirconium oxide, yttrium oxide, barium strontium titanium oxide, and silicon nitride.

18. The transistor of claim 9, wherein the gate electrode comprises at least one of titanium nitride, tantalum nitride, titanium, tantalum, nickel, platinum, polygermanium, and polysilicon.

19. A device comprising:

a semiconductor substrate, the substrate being substantially free of silicon;

a well formed in a portion of the substrate, the well having a first type of dopant;

a gate dielectric layer formed over a portion of the well;

a gate electrode defined over a portion of the gate dielectric layer; and

a source region and a drain region defined proximate the gate electrode in the well, the source and drain regions being defined by a second type of dopant.

20. The device of claim 19, wherein the first dopant is n-type and the second dopant is p-type.

21. The device of claim 19, wherein the first dopant is p-type and the second dopant is n-type.